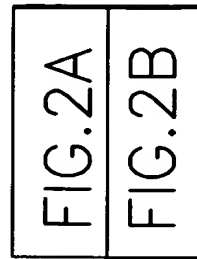
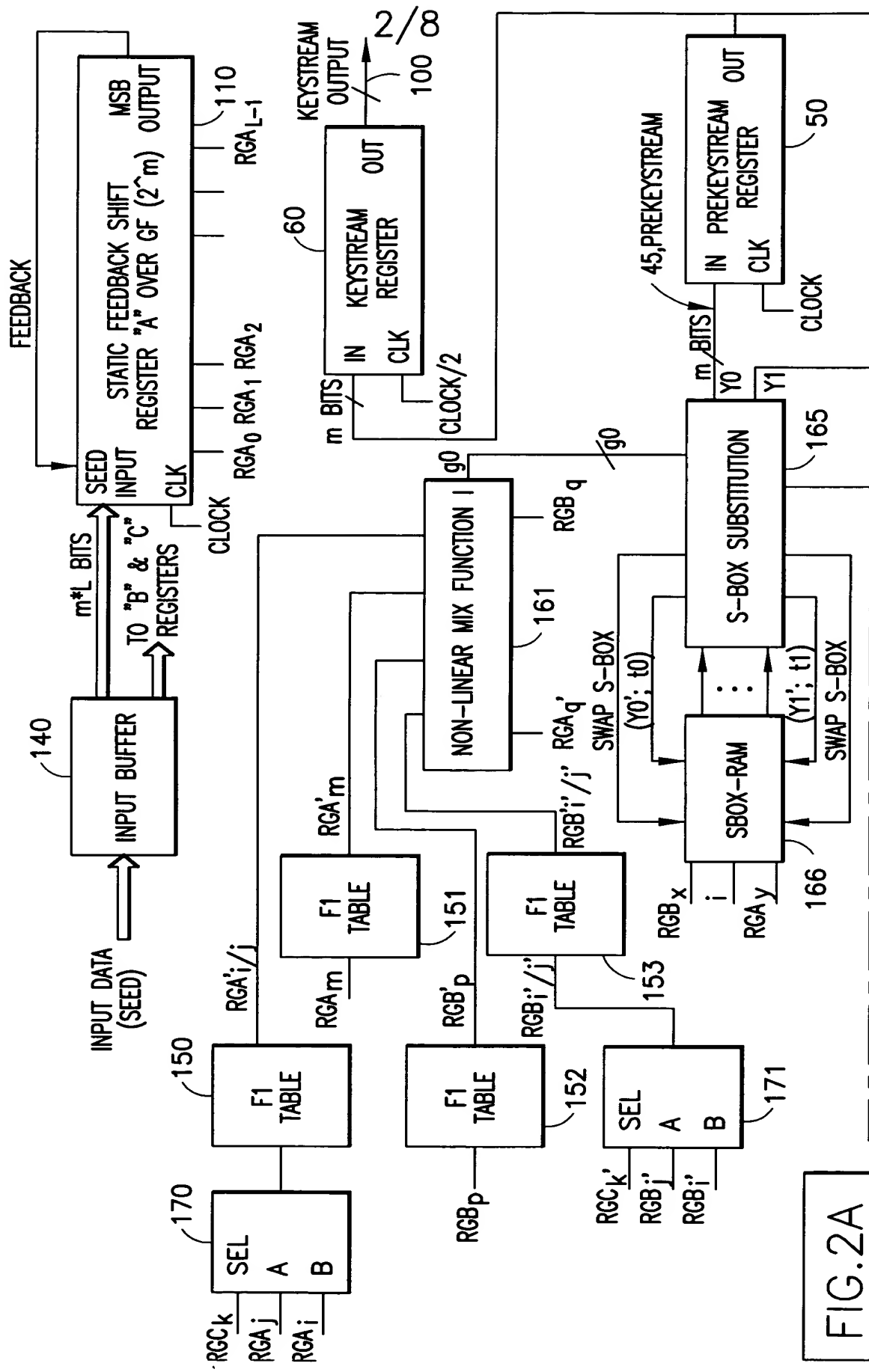


FIG. 1



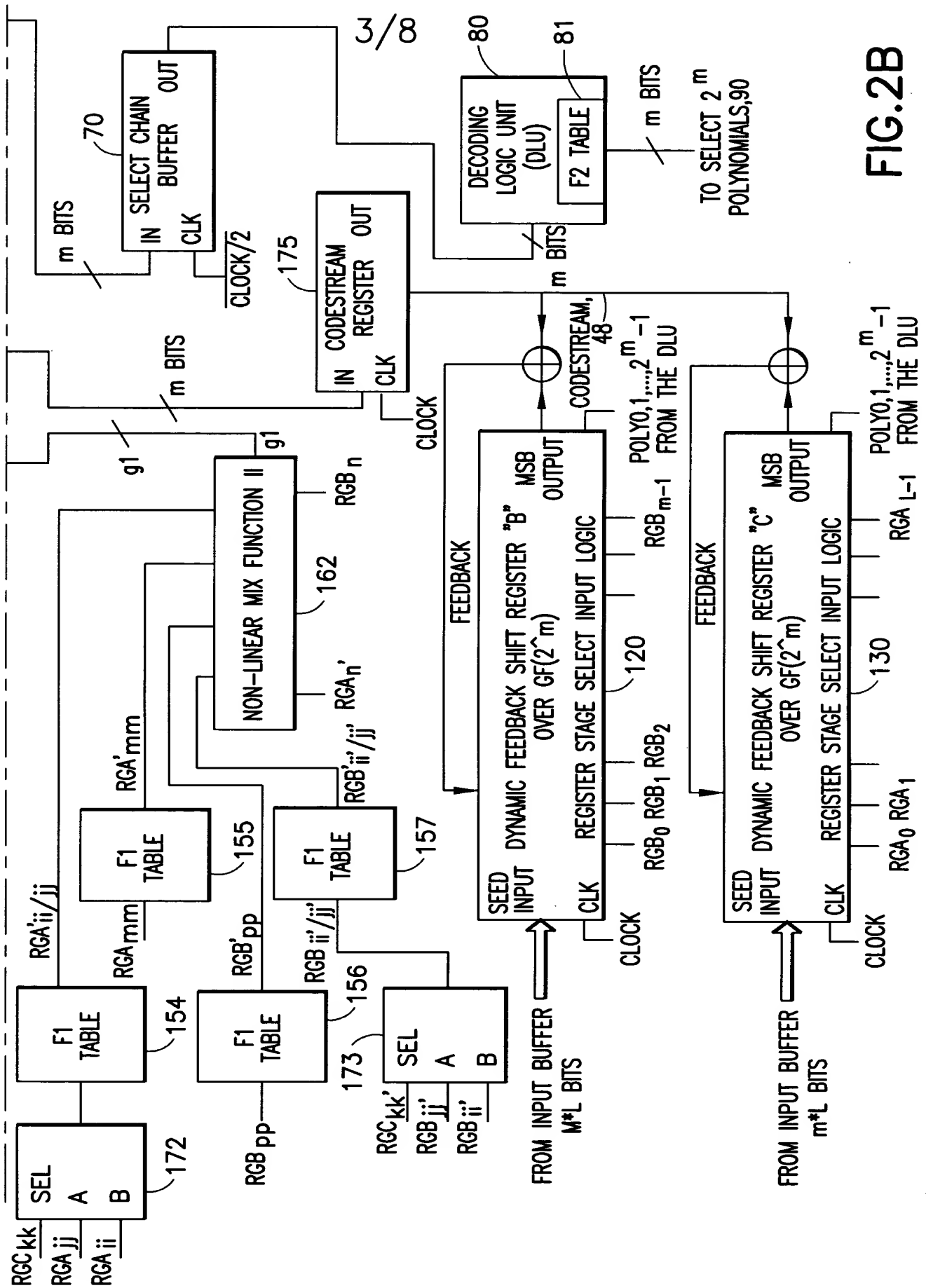


FIG. 2B

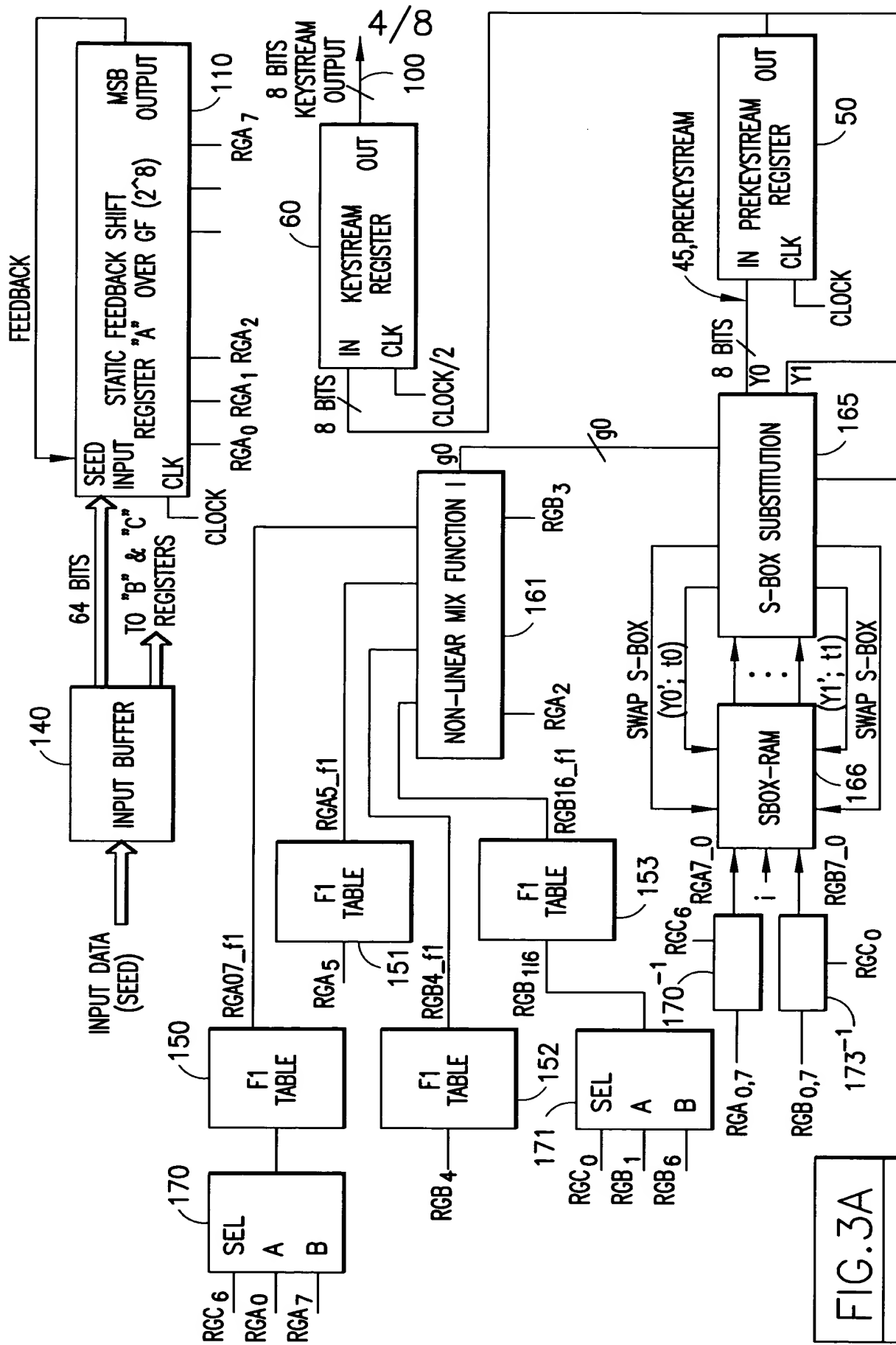


FIG. 3A

FIG. 3

FIG. 3B is a block diagram of a video processing system, such as a video encoder or decoder, for processing video data. The system includes a video input buffer, a video processing unit, and a video output buffer. The video processing unit includes a video input register, a video processing block, and a video output register. The video input register receives video data from the video input buffer and outputs video data to the video processing block. The video processing block processes the video data and outputs video data to the video output register. The video output register outputs video data to the video output buffer. The video processing block includes a video input register, a video processing block, and a video output register. The video input register receives video data from the video input buffer and outputs video data to the video processing block. The video processing block processes the video data and outputs video data to the video output register. The video output register outputs video data to the video output buffer.

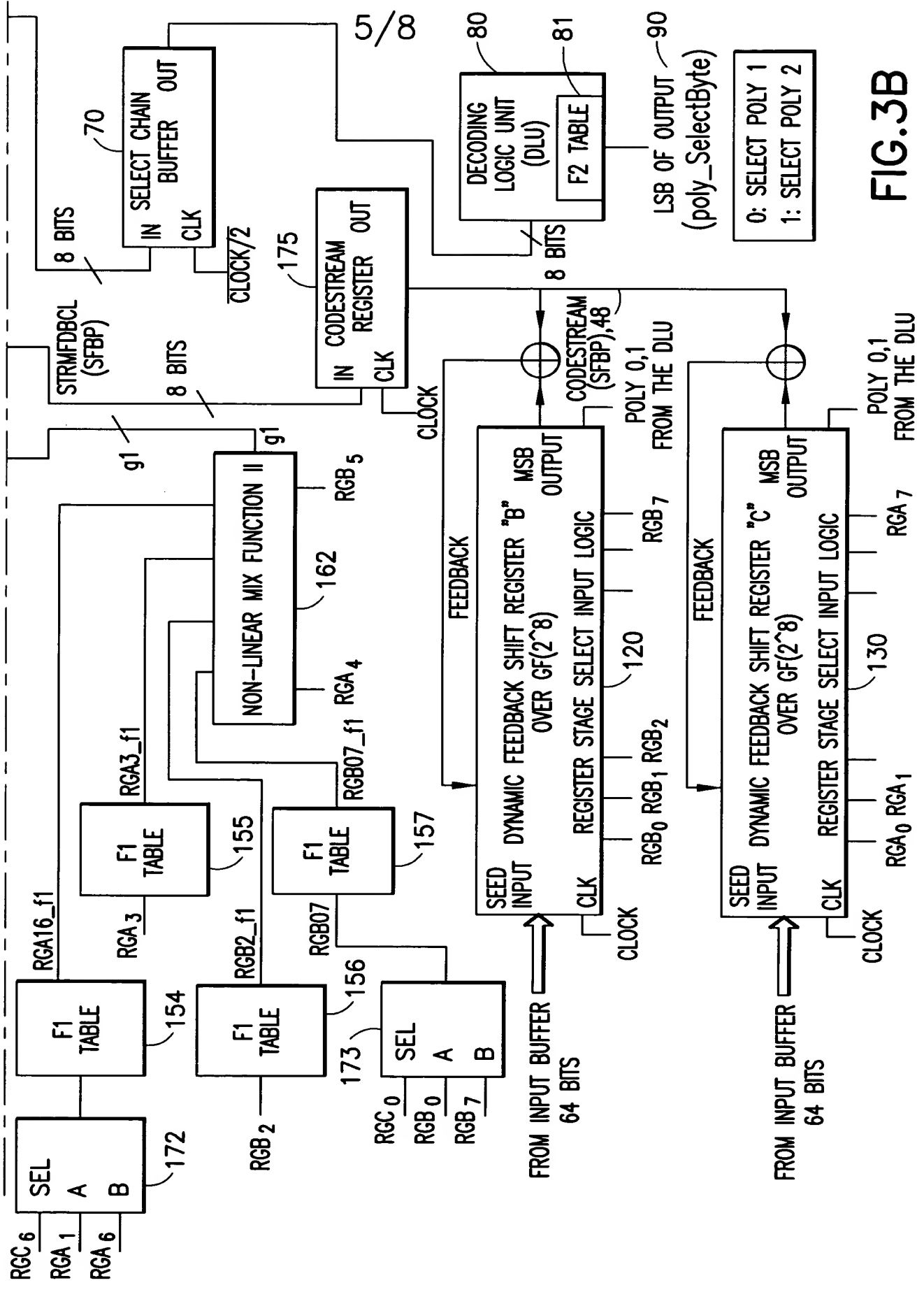


FIG. 3B

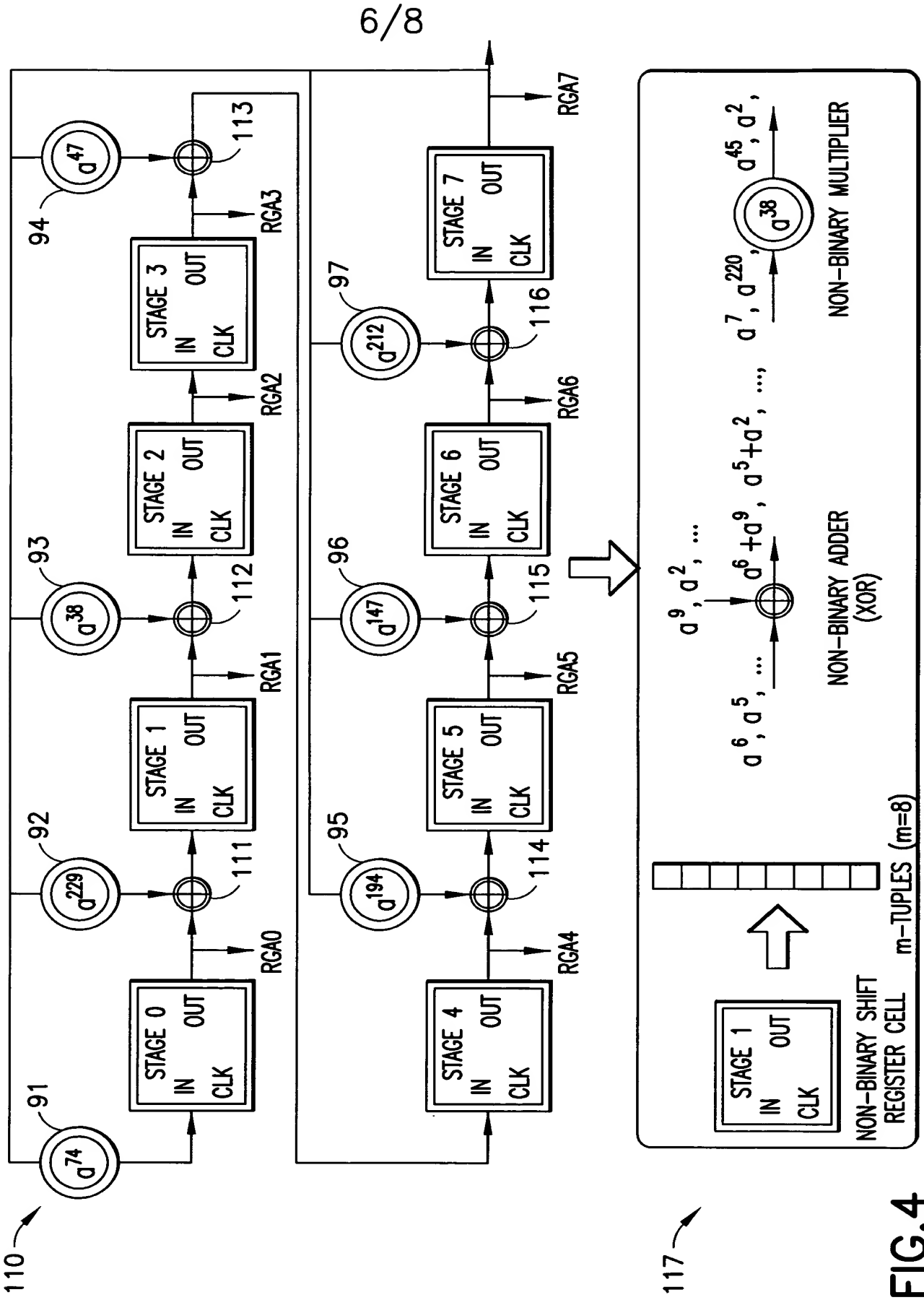


FIG. 4

FIG. 5 is a block diagram of a multi-stage pipeline for processing digital data. The pipeline consists of seven stages, each containing a 2-to-1 multiplexer and a 2-to-1 adder. The stages are labeled STAGE 0 through STAGE 7. The input to STAGE 0 is a 2-bit value (0 or 1) and a 2-bit value (0 or 1). The output of STAGE 0 is a 2-bit value (0 or 1). The output of STAGE 1 is a 2-bit value (0 or 1). The output of STAGE 2 is a 2-bit value (0 or 1). The output of STAGE 3 is a 2-bit value (0 or 1). The output of STAGE 4 is a 2-bit value (0 or 1). The output of STAGE 5 is a 2-bit value (0 or 1). The output of STAGE 6 is a 2-bit value (0 or 1). The output of STAGE 7 is a 2-bit value (0 or 1).

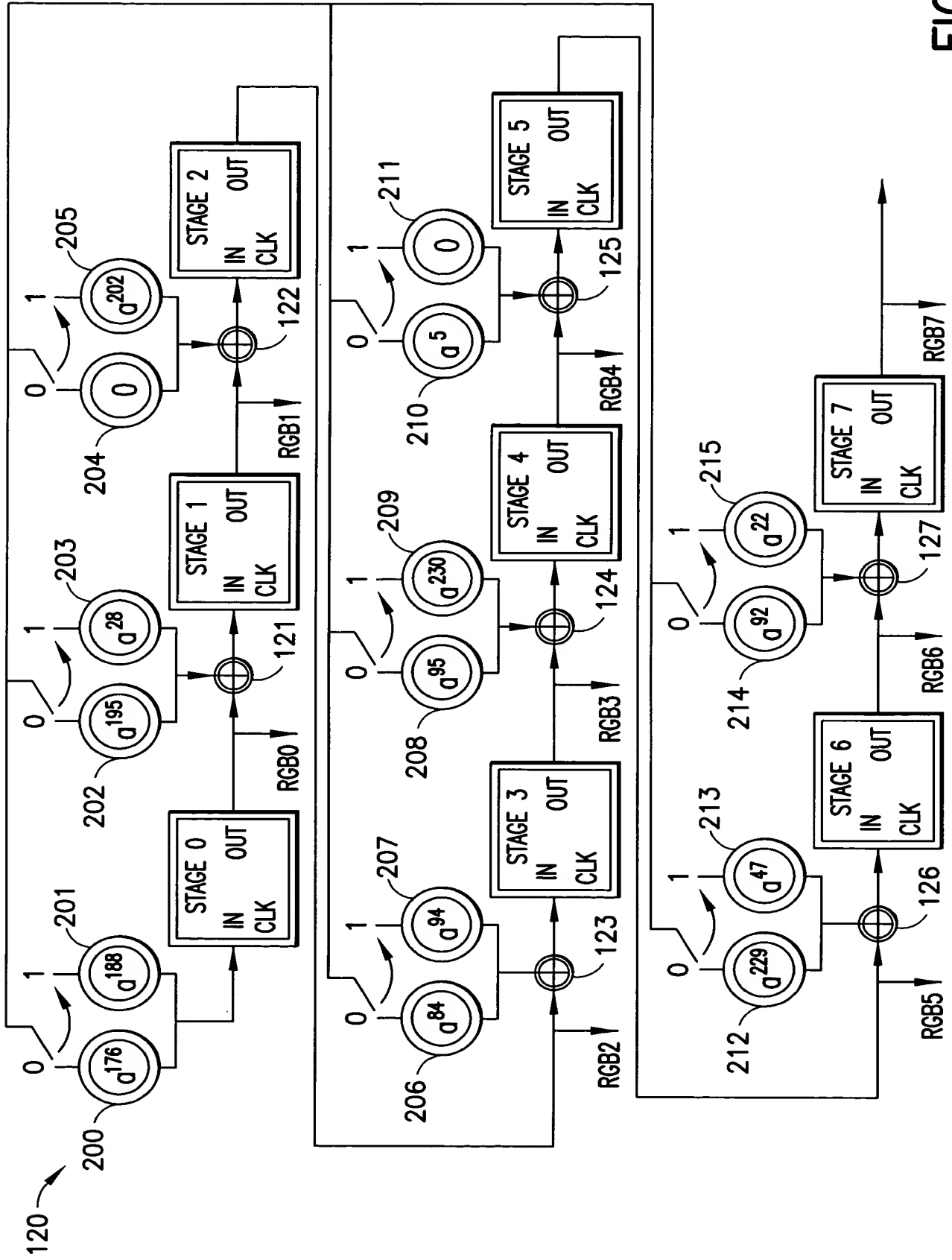


FIG.5

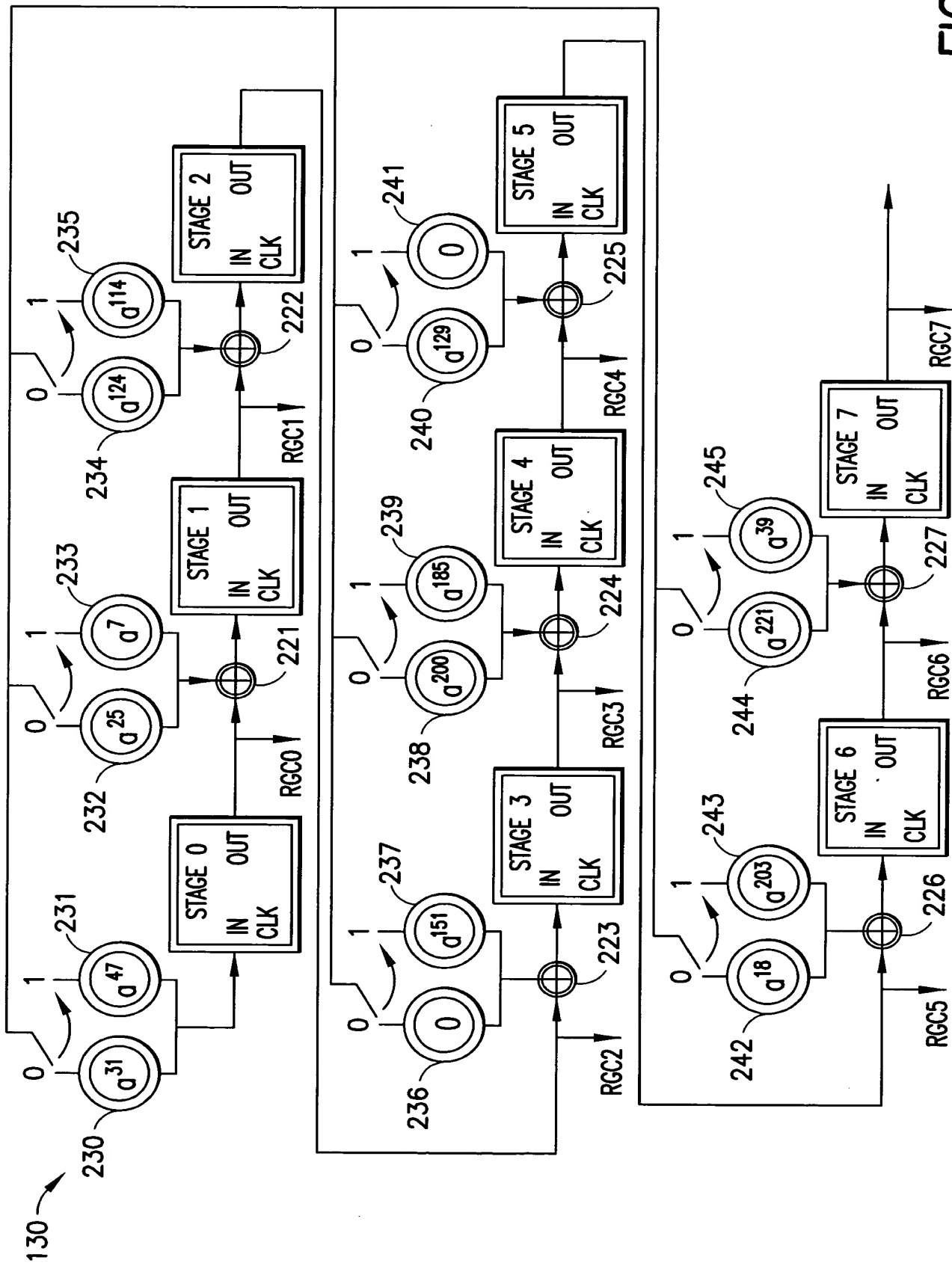


FIG. 6